IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 4, Issue 9, September 2016

Simulation of a Cascaded Multilevel Inverter Topology with Reduced Number of Switches

Manoj Siva Kumar K[1], Jayadurga B[2]

(Ph.D), Dept of Electrical Engineering, VITS, Kavali, India[1]

M.Tech, Dept of Electrical Engineering, VITS, Kavali, India[2]

Abstract: This paper proposes a topology of a cascaded multilevel inverter that utilizes less number of switches than the conventional topology. Therefore with reduced number of switch count topological structures configured in the form of a matrix for a cascaded Multi level inverter (CMLI). As the numbers of switches are reduced, both conduction and switching losses will be decreased and electromagnetic interference is reduced, which leads to increase the efficiency of converter. The proposed inverter focus extends to produces number of voltage levels in the same number of the voltage source and reduced number of switches compared to the conventional inverters. Thus the inverter will be simulated with the implementation of appropriate pulse width modulation (PWM) techniques strategy to generate firing pulses and ensure the desired operation of the power modules techniques and its effect on the harmonic spectrum will be analyzed. The system will be modeled with the help of MATLAB/SIMULINK

Keywords: Cascaded multilevel inverter, Matrix topology, PWM Strategy.

1. INTRODUCTION

Since several years, there has been a growing demand for medium and high voltage power conversion systems. Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on.

The cascade multilevel inverter was first proposed in 1975 [6]. Separate DC-sourced full-bridge cells are placed in series to synthesize a staircase AC output voltage. The term multilevel began with the three-level converter [7]. Subsequently, several multilevel converter topologies have been developed [8]. The advantages of cascade multilevel inverters were prominent for motor drives and utility applications. The cascade inverter has drawn great interest due to the great demand of medium-voltage high-power inverters.

The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed.

Abundant modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. In this modeling sinusoidal pulse width modulation (SPWM) is used.

2. MULTILEVEL INVERTERS

Switched mode inverters find wide applications in power industry. These inverters require control of both the magnitude and frequency of an ac output. Practically, inverters are used in both single phase and three phase AC systems. A half bridge inverter is the simplest topology, which is used to produce a two level square wave output waveform. A center tapped voltage source supply is needed in such a topology. On the other hand, the full bridge topology is used to synthesize both three level and two level output waveforms.

However, the above mentioned inverters have limitations in handling high voltage and high power conversion. For higher output voltage capacity and reduction in harmonic distortion, these converters need to be connected in series using transformers. Also, these series connection of inverters are the contributors to problems such as bulkiness, high loss and high cost to the overall AC system. Besides that, conventional inverters have some disadvantages operating at high frequency mainly due to switching losses and constraints of the device ratings.

To overcome the disadvantages of conventional inverters, multilevel inverters emerge as the new breed of converters in high and medium power applications. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells.

Types of Multilevel Inverters

Multilevel inverter topologies are classified into three types:

1. Diode clamped multilevel inverter,
2. Flying capacitor multilevel inverter and
3. Cascaded H-bridge multilevel inverter.

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 4, Issue 9, September 2016

In diode clamped multilevel inverter a bank of series connected capacitors will divide the dc link voltage into small steps. Inverter poles can be connected to any one of these voltage steps to generate the complete multilevel output.

Flying capacitor multilevel inverter consists of pre charged capacitors and this capacitor voltage is added or subtracted from the dc voltage to obtain the required levels.

Cascaded H bridge multilevel inverter includes a number of single phase H bridges connected in series, the output of which is equal to the sum of voltage produced by each bridge.

3. CMLI TOPOLOGY

The main abstraction is to offer various levels of output voltages by erupting up with a generalized structure for a single phase CMLI.

In this structure a key philosophy involves where the power switches are arranged in the form of a matrix structure (axb) and the arrangement of voltage sources in order to obtain different output levels.

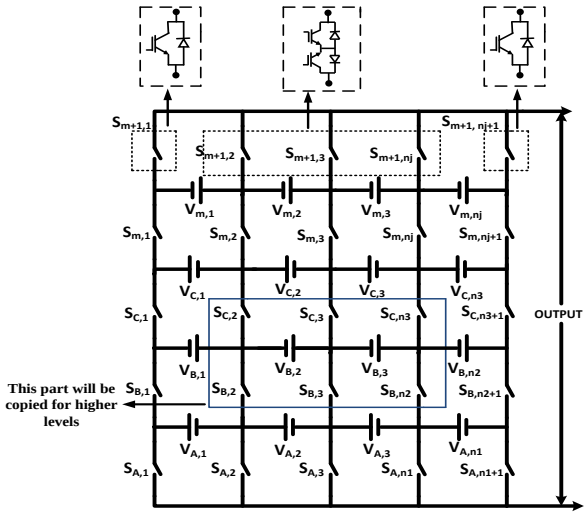


Fig.1. Generalized structure

The generalized structure shown in Fig.1 Quaff voltage sources (VA,1-VA,n1), (VB,1-VB,n2), (VC,1-VC,n3), (Vm,1-Vm,nj) arranged in each row , thus arranged voltage sources are isolated from each other and those connected in series in the design . For renewable energy sources such as energy storage devices or photovoltaic cells or fuel cells [10-11].

The architecture contains the switches in the matrix in this front line switches (SA,1-SA,n1+1),(Sm+1,1 - Sm+1, ,nj+1) encompasses the top and bottom of the circuit and the voltage sources are connect to the load by the intermediate switches (SB,1-SB,n2+1), (SC,1-SC,n3+1), (Sm,1-Sm,nj+1).

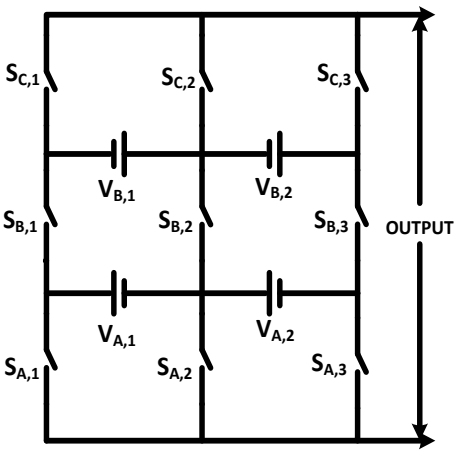


Fig.2. nine level topology

With four isolated dc switches the schematic of nine level inverter topology is shown in the Fig.2.Where it uses only 12 switches to produce the nine level when compared to the conventional topology. For the sense to produce the output voltage of (VA,1 and VA,2) we need to conduct (SA,1, SB,1 and SA,3).In the view of presence of the voltage source (VA,2) the body diode in the device (SA,2) is forward biased, where it explode to create inter-looping problem. To avoid inter-looping problem we are going to use bi-directional devices. Several bi-directional configurations has been proposed, but we are using common emitter configuration in the proposed topology. So to protect the voltage source from the inter-looping problem these are apt only in the intermediate column. In order to obtain the higher voltage levels the middle stage as represented in the Fig.1 can be two folded.

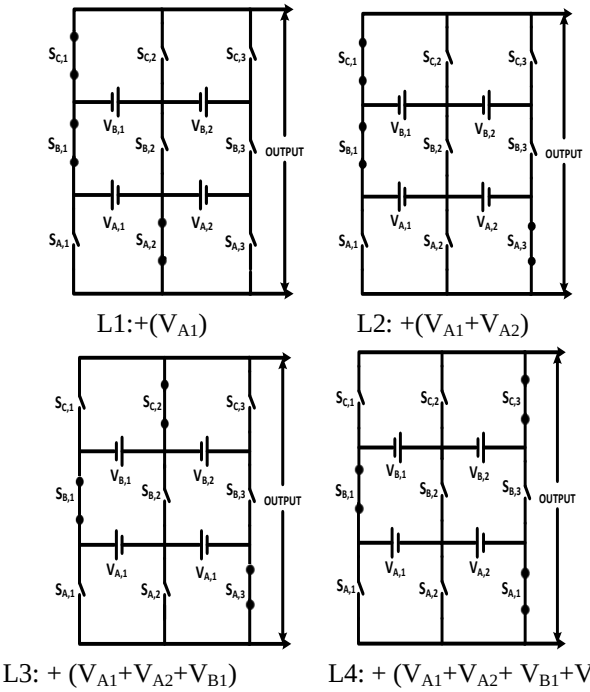


Fig.3. Operation of Positive mode

DOI 10.17148/IJIREEICE.2016.4935

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 4, Issue 9, September 2016

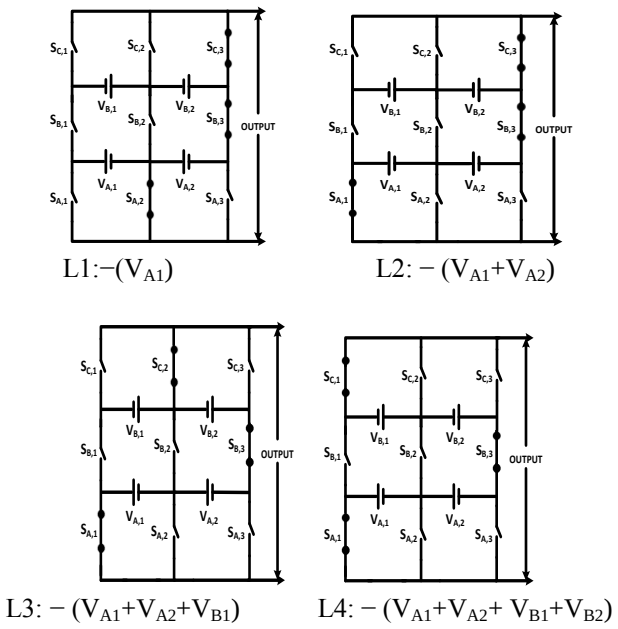


Fig.4. Operation of Negative mode

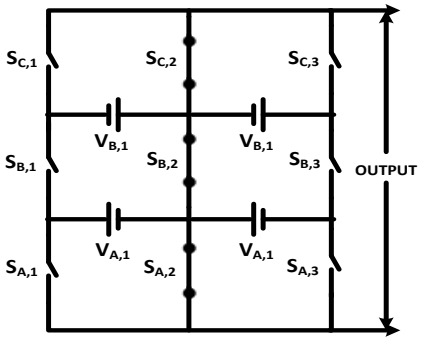


Fig.5. Operation of Zero mode

The operation modes for the proposed schematic nine level inverter topology involves three modes. This three modes of operation shown in Fig.3 to Fig.5 has subtlety in the methodology and transcend realities in the formulation. In the mode-1 in the order to obtain output voltage switches SA,2 ,SB,1, SC,1 are on. From the Fig.3 to Fig.5 it can be clearly observe the operational pattern where the output voltage is obtained only when the three devices are switched and from this we are going to decrease the switching power dissipation due to the minimal switching transition during each mode of transfer.

Table 1. PWM signals to obtain positive level output voltage

PWM Signals	Positive Output Levels	Signals gated to the switches
PWM 1	Positive Level 1	S A,2 , S B,1 , S C,1
PWM 2	Positive Level 2	S A,3 , S B,1 , S C,1
PWM 3	Positive Level 3	S A,3 , S B,1 , S C,2
PWM 4	Positive Level 4	S A,3 , S B,1 , S C,3

Table 2. Comparison of power components for single phase 9 level inverter between conventional topologies and proposed topologies

Power Components	Diode Clamped	Flying Capacitor	Cascaded	Proposed
Main Switches	16	16	16	12
Main Diodes	16	16	16	12
Gate Drivers	16	16	16	9
Clamping Diodes	56	0	0	0
Flying Capacitors	0	28	0	0
DC-link Capacitors	4	4	4	4
Total	108	80	52	37

Table 1 present how to extract different output voltage levels by using the PWM signals here it represents only for the positive output voltage, while similar arrangement are made to produce PWM single for negative cycle. The values in Table 2 compare the conventional and proposed topologies, requirements of the power components in order to produce the required nine level output is given by ((2× (a×b))+1 level . To obtain the different levels using the proposed topology for single/three phase it ingress in Table 3 represents the requirement of number of switches in conduction path, gate drivers, power switches and DC sources thus it corroborate the merits of the proposed topology.

Table 3. Required power components for proposed topology for single phase and three phase

Power Components	Single phase components	Three phase components
Main Switches	(2 x b) x (a+1)	(6 x b) x (a+1)
Main Diodes	(2 x b) x (a+1)	(6 x b) x (a+1)
Gate Drivers	(a+1) x (b+1)	3 x (a+1) x (b+1)
Clamping Diodes	--	--
Flying Capacitors	--	--
DC-link Capacitors	(a x b)	3 x (a x b)
Devices in conduction path	(a+1)	3 x (a+1)

4. MATLAB/SIMULATION RESULTS

To show the performance of the proposed cascaded converter, the focus is on modelling and simulation of single phase inverter modulated by Phase Disposition Sinusoidal Pulse Width Modulation (PD-SPWM). Phase Disposition Sinusoidal Pulse Width Modulation is a

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 4, Issue 9, September 2016

technique that use as a way to decrease total harmonic distortion in inverter circuit. The model is implemented using MATLAB/Simulink software with the Sim Power System Block Set based on computer simulation. In the acknowledged topology, the switching operation is separated into high- and low-frequency elements. The essential advantages are minimize whole Harmonic Distortion (THD), much less stress on the energy switches and greater efficiency. The predominant disadvantage is the excessive number of power switches which makes the control method problematic and for this reason excessive fee. This paper presents a nine level inverter utilizing less number of switches. This may occasionally add up to the efficiency of the converter as well as reducing the scale and cost of the ultimate prototype. The feasibility of the proposed technique is validated making use of laptop simulations. A model of the nine-stage inverter is constructed in MATLAB-Simulink application. A new method with diminished number of switches is employed. The proposed topology and it's manipulate approach are explained and unique simulation has been applied in MATLAB/Simulink. Simulation of the proposed topology of multilevel inverter is performed utilizing Matlab.

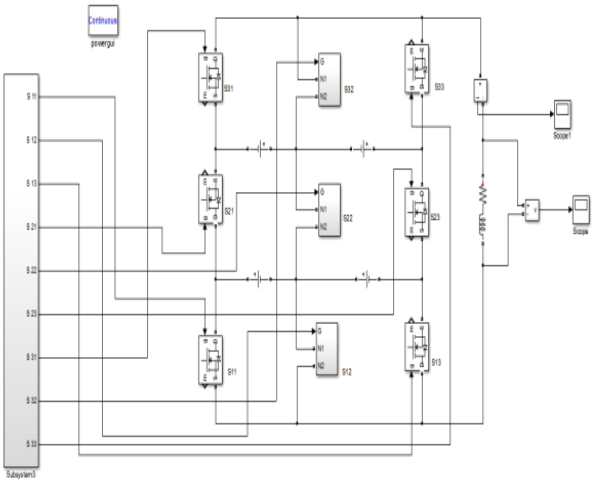
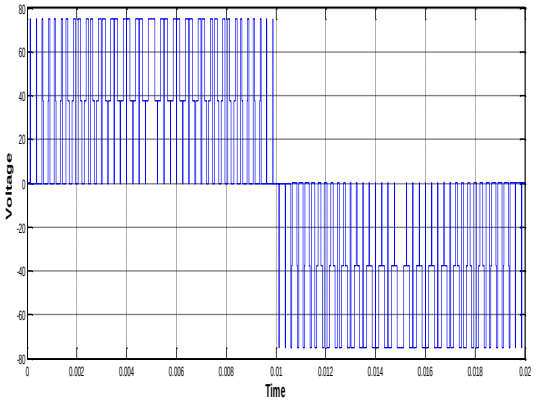


Fig.6. Matlab/Simulink model of single-phase nine level multilevel inverter with proposed pd-spwm

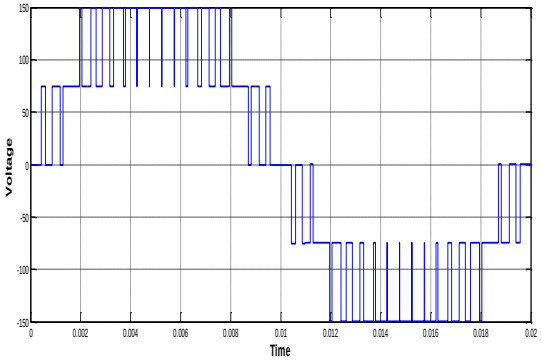
Simulation is done for three, five, seven, nine levels .THD and the load currents with RL load is observed. With increase in number of levels THD is reduced. Voltage, THD and Current waveforms with different levels are given in Fig7 to Fig9.

Table.4. Show the comparison of T.H.D for different levels

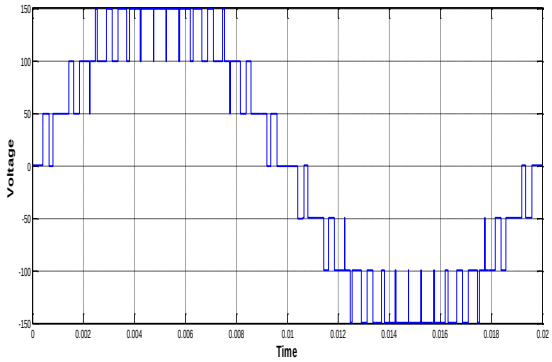
Sl. No.	No. Of Levels	T.H.D
1.	Three level	41.58
2.	Five level	25.60
3.	Seven level	17.19
4.	Nine level	12.36



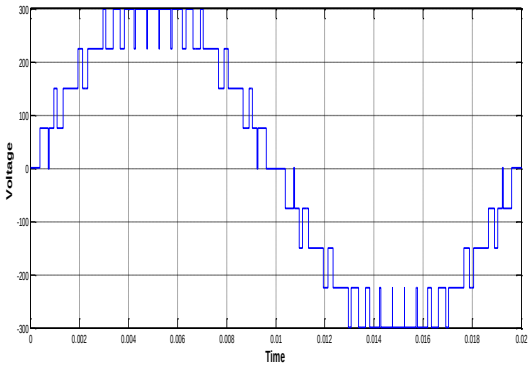
(a) three level



(b) five level



(c) seven level



(d) Nine level

Fig.7. Output voltages for: (a) three level (b) five level (c) seven level (d) nine level

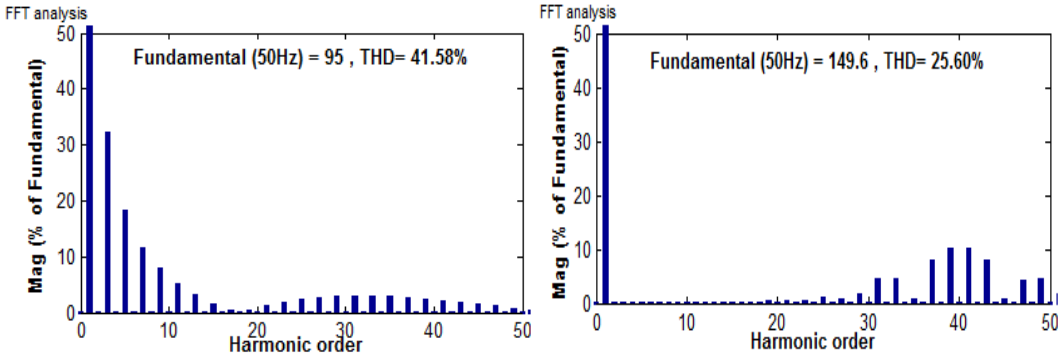
IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

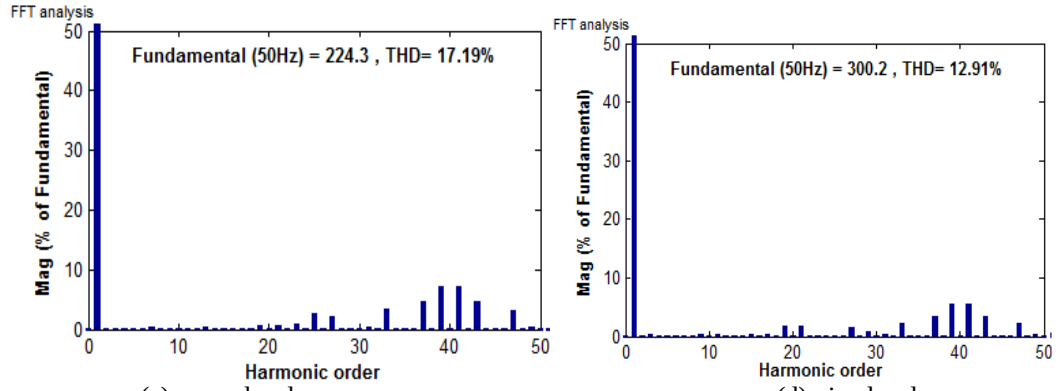
International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 4, Issue 9, September 2016

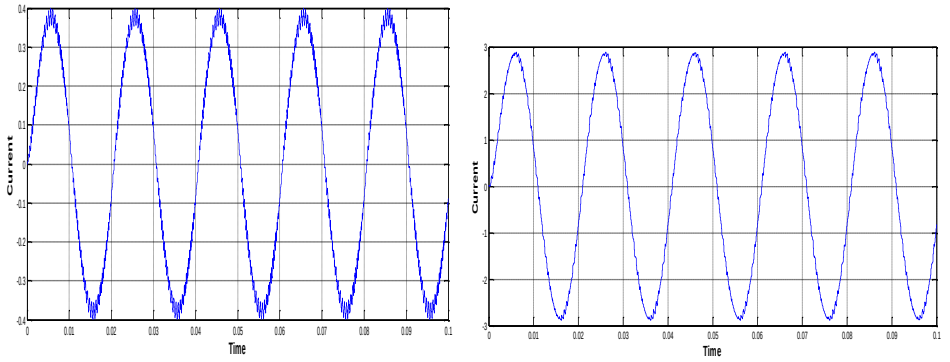


(a) Three level (b) five level

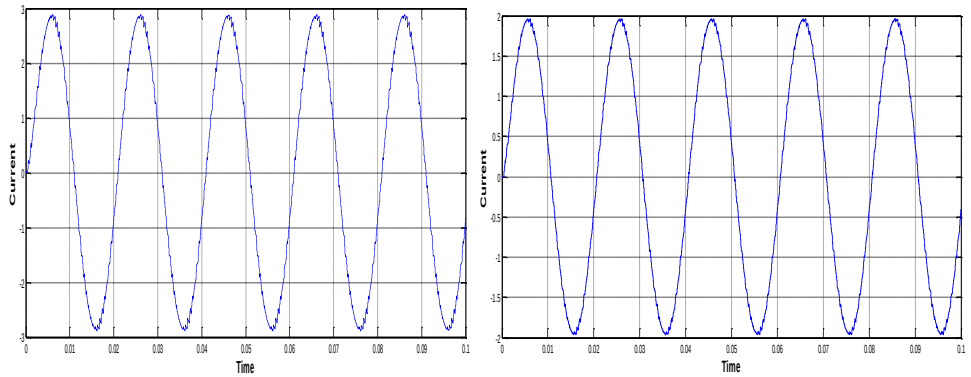


(c) seven level (d) nine level

Fig.8. FFT Analysis for: (a) three level (b) five level (c) seven level (d) nine level



a) Three level b) Five level



c) Seven level d) Nine level

Fig.9. Single phase inductive load current : (a) three level (b) five level (c) seven level (d) nine level

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 4, Issue 9, September 2016

The circuit diagram constructed for 9-level are simulated for load R-L. From that, we get voltage and current waveforms are exposed in the above figures. The modelling of multilevel inverter was done and simulated using Simulink. Matlab-Simulink models of a single phase nine level inverters is developed and output voltage and current waveforms are observed for RL loads. The switching pulses are resulting based on phase disposition of sinusoidal pulse width modulation. In phase disposition sinusoidal Pulse Width Modulation, all the carrier waveforms are in phase.

The total harmonic distortion is very low compared to that of classical inverter. The simulation result shows that the harmonics have been reduced. The multilevel inverter system has been successfully simulated and the results of voltage waveforms, current waveforms, and number of switches in the conduction path are compared for both convection as well as for proposed.

5. CONCLUSION

This paper thrive about the CMLI topology structure arranged in a matrix order. The topology has shown that the CMLI had produce the output voltage with less number of the power switches when compared to the convectional CMLI. The main advantage of the proposed structure is the number of switching devices as well as the gate drives are reduced therefore the circuit becomes less complex for control, the size and cost are reduced. In this topology the conduction period is desperately get reduced for switching modes of operation, thus which reduced the conduction losses and electromagnetic interference. To evaluate the operation of proposed topology simulation results have provided that proposed inverter produce less harmonic distortion when compared to the conventional CMLI. This generalized topology can be extended to higher levels by duplicating the intermediate switches.

REFERENCES

[1] Ebrahim Babaei. "A Cascade Multilevel Converter Topology With Reduced Number of Switches". IEEE Trans. On Power electronics. 2008; 23(6): 2657-2664.

[2] Jacob James Nedumgatt, Vijayakumar D, A Kirubakaran, Umashankar S. A Multilevel Inverter with Reduced Number of Switches. IEEE Students' Conference on Electrical, Electronics and Computer Science. 2012.

[3] Seyed Hossein Hossein,Amir Farakhor,Saeideh Khadem Haghighian, "New Cascaded Multilevel Inverter Topology with Reduced Number of Switches and Sources"

[4] José Rodríguez,Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies,Controls, and Applications". IEEE Transactions On Industrial Electronics, Vol. 49, No. 4, August 2002

[5] Mariusz Malinowski, K. Gopakumar, Jose Rodriguez, and Marcelo A. Pérez, "A Survey on Cascaded Multilevel Inverters". IEEE Transactions On Industrial Electronics, Vol. 57, No. 7, July 2010.

[6] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "A comparative analysis between the symmetric and the hybrid asymmetric nine-level series connected H-bridge cells inverter," in Proc. Eur. Conf. Power Electron. Appl., 2007, pp. 1-10.

[7] M. R. Banaei and E. Salary, "A New Family of Cascaded Transformer Six Switches Sub-Multilevel Inverter with Several Advantages"

[8] Ritu Chaturvedi, Praveen Bansal, "A Series-Parallel Switched Reduced Devices Multilevel dc-link Inverter Topology" International Journal of Science, Engineering and Technology Research (IJSETR), Volume 3, Issue 5, May 2014

[9] Brendan Peter McGrath and Donald Grahame Holmes, "Multicarrier PWM Strategies for Multilevel Inverters" IEEE Transactions On Industrial Electronics, Vol. 49, No. 4, August 2002

[10] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for dc-ac conversion," IEEE Trans. Power Electron., vol. 21, no. 5, pp. 1311-1319, Sep. 2006

[11] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Singlephase seven-level grid-connected inverter for photovoltaic system," IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2435-2443, Jun. 2011

[12] Tengfei Wang and Yongqiang Zhu, "Analysis and Comparison of Multicarrier PWM Schemes Applied in H-bridge Cascaded Multi-level Inverters"

BIOGRAPHIES

Manoj Siva Kumar K (Ph.D), Dept of Electrical Engineering, VITS, Kavali, India

Jayadurga B (M.Tech), Dept of Electrical Engineering, VITS, Kavali, India